

Graceful **Failure** *Recovery*— The NSF CAREER Pursuit

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NSF CISE CAREER Workshop – April 29

josiahhester.com



(Ambitious) Agenda

KA MOAMOA

- Me (short)
- My Timeline
- Developing a CAREER vision
- Zoom-in, walk through my CAREER
- Best (?) practices

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No way can I cover everything here...

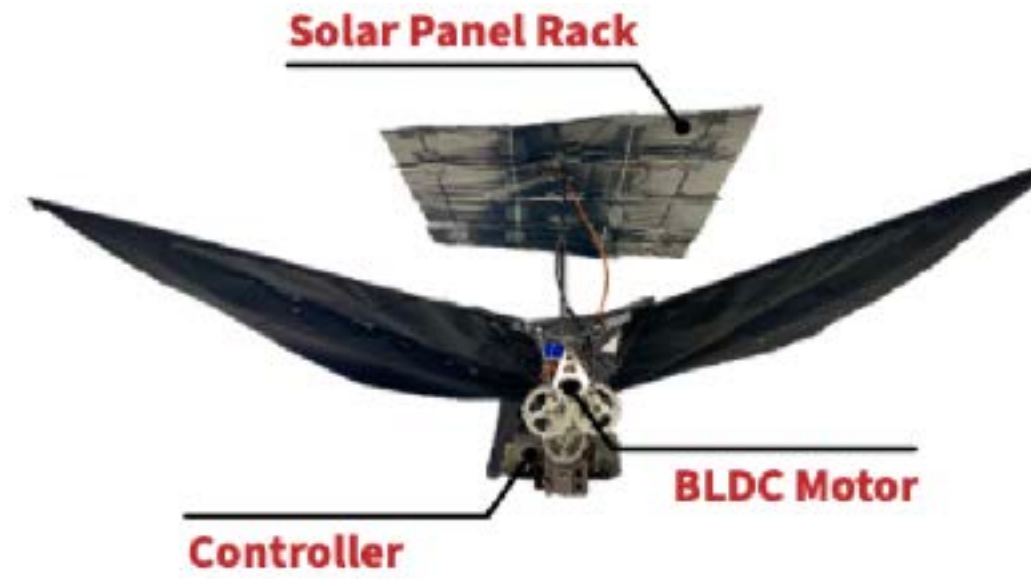


Batteries are ecologically harmful, and reduce system lifetime!

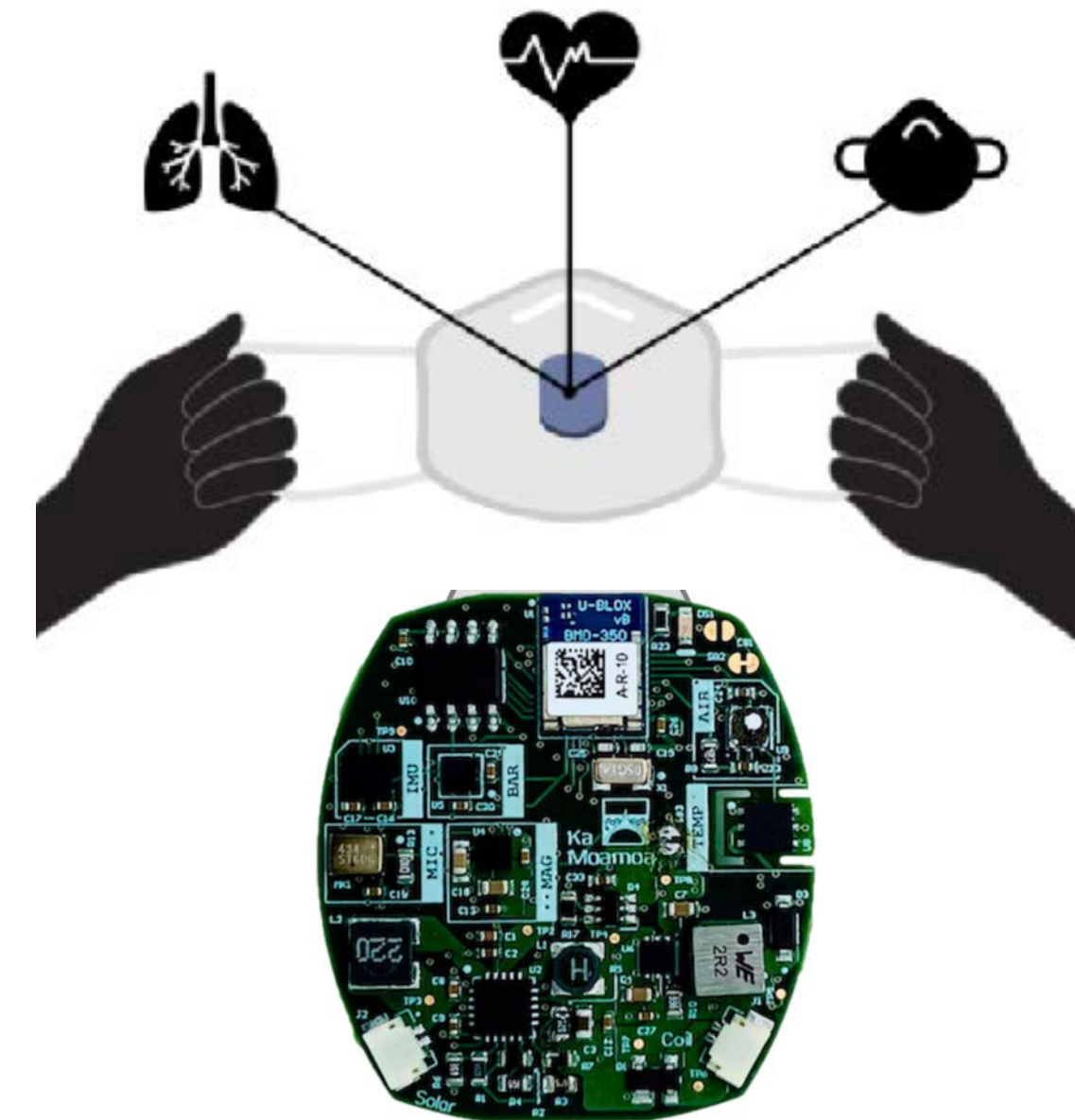
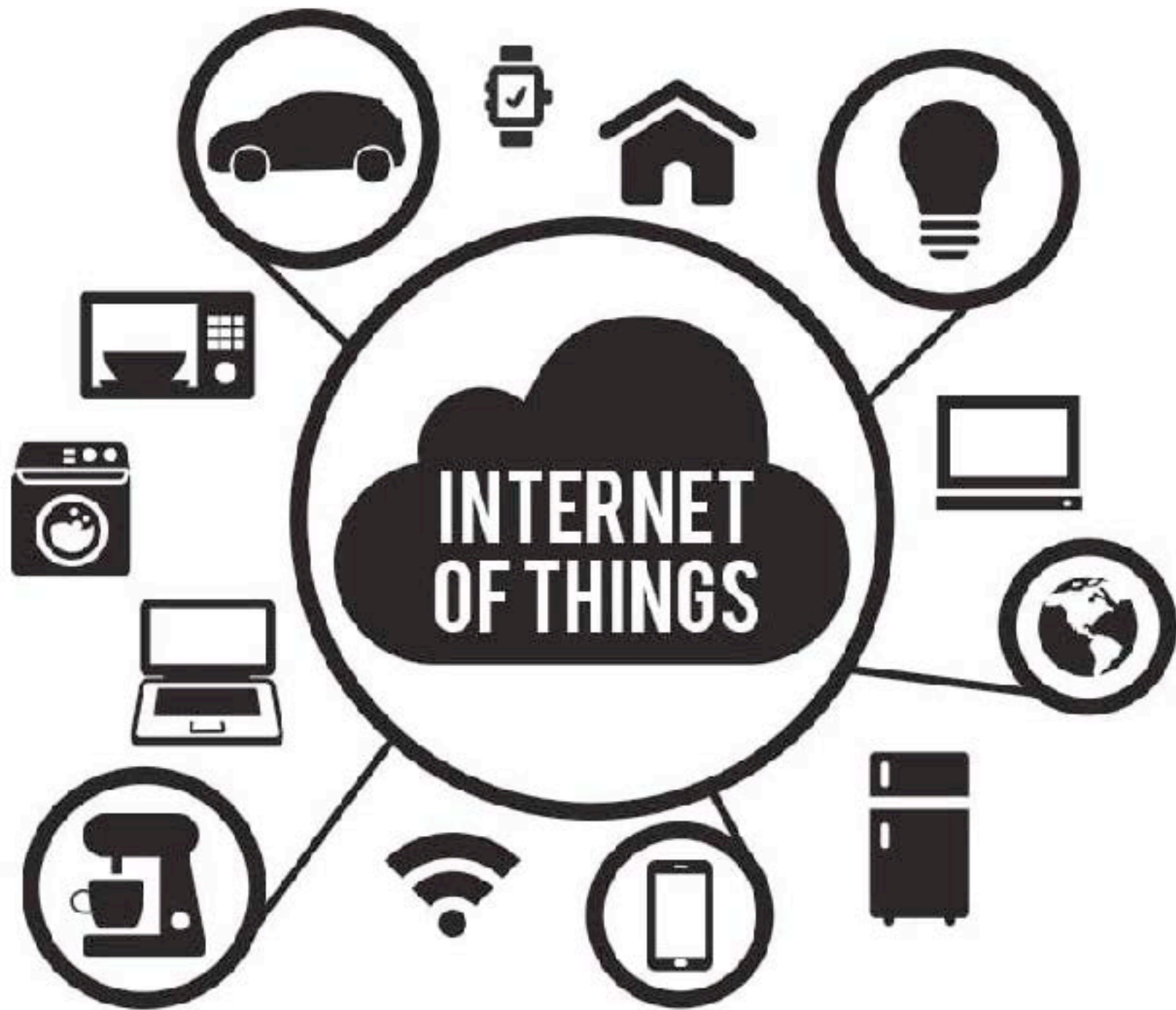


Can we harvest energy needed from our environment instead?





What is it **good** for?

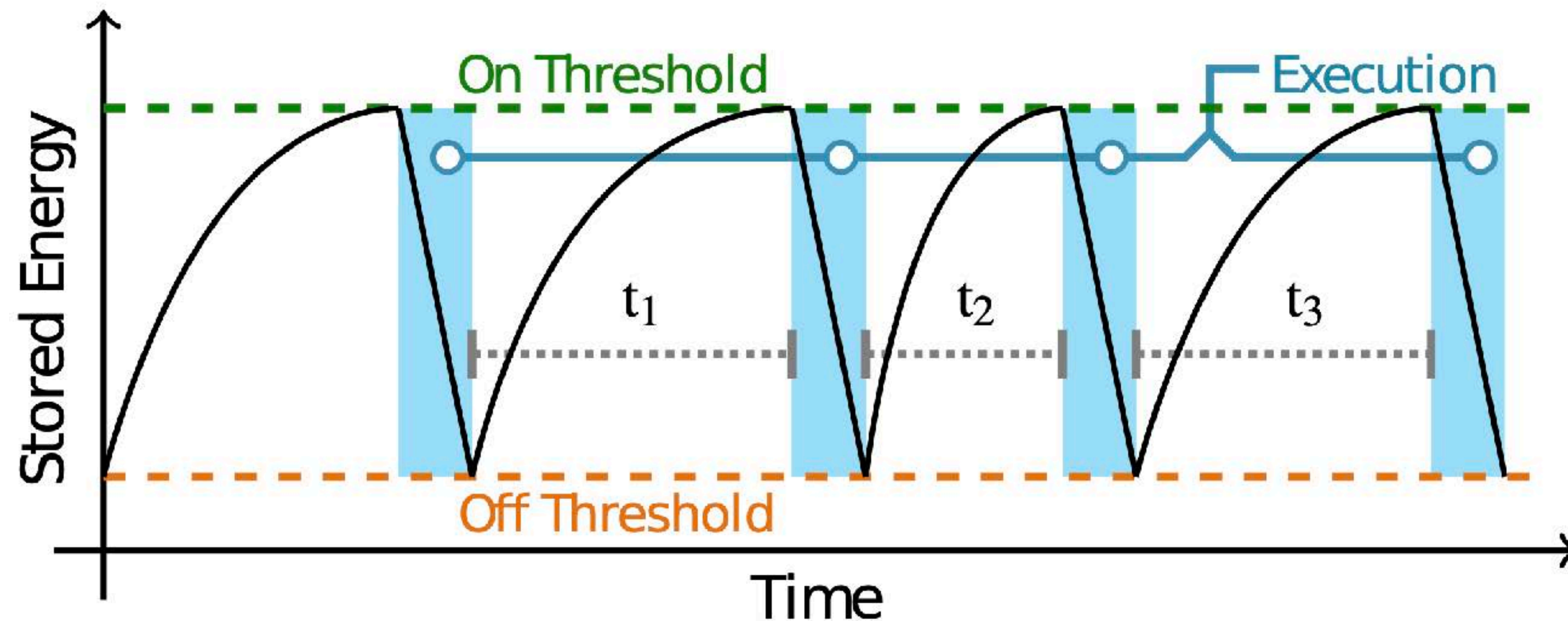


Power Failures: Intermittent Computing

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So little energy storage, dynamic power input...

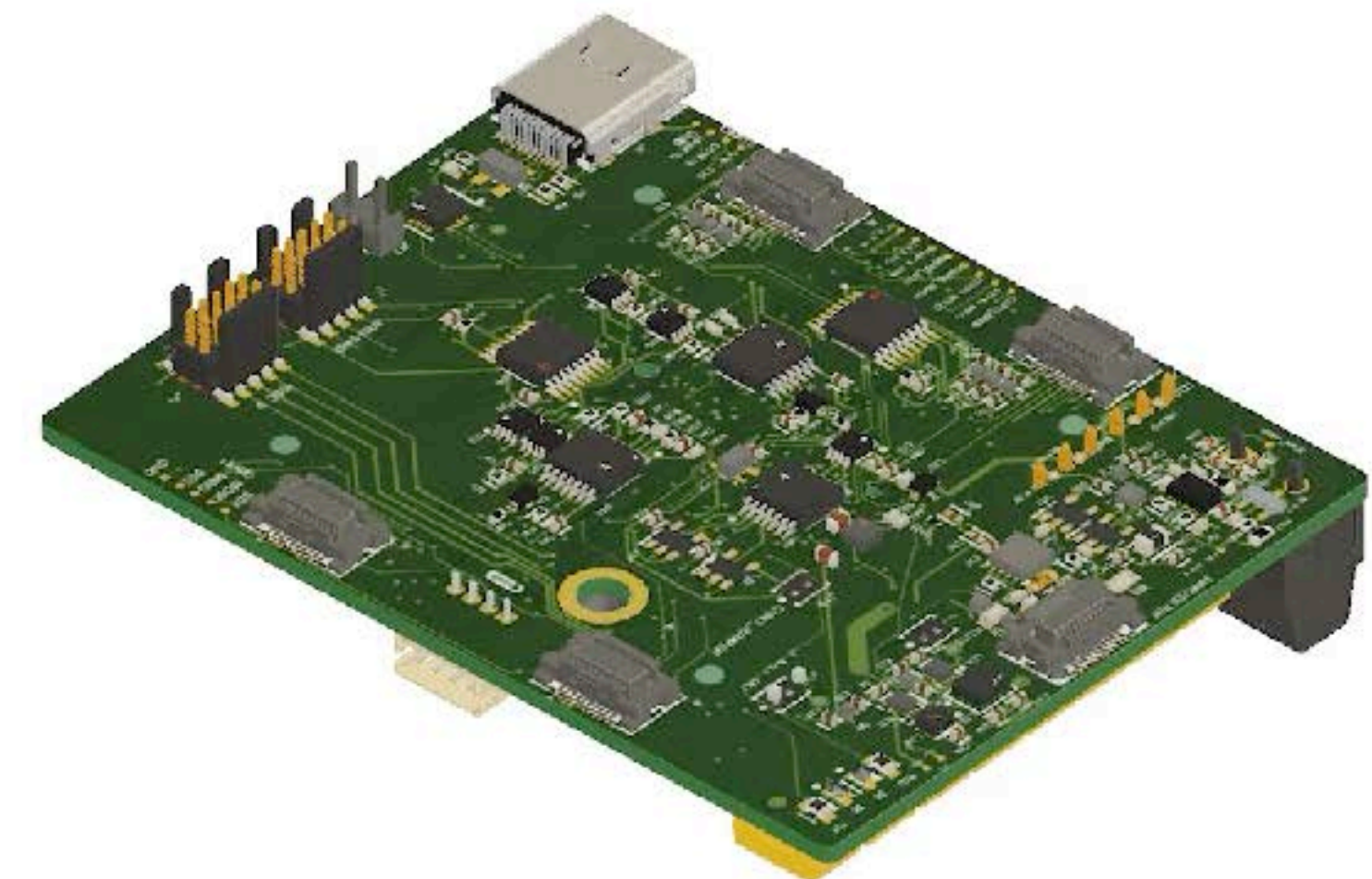
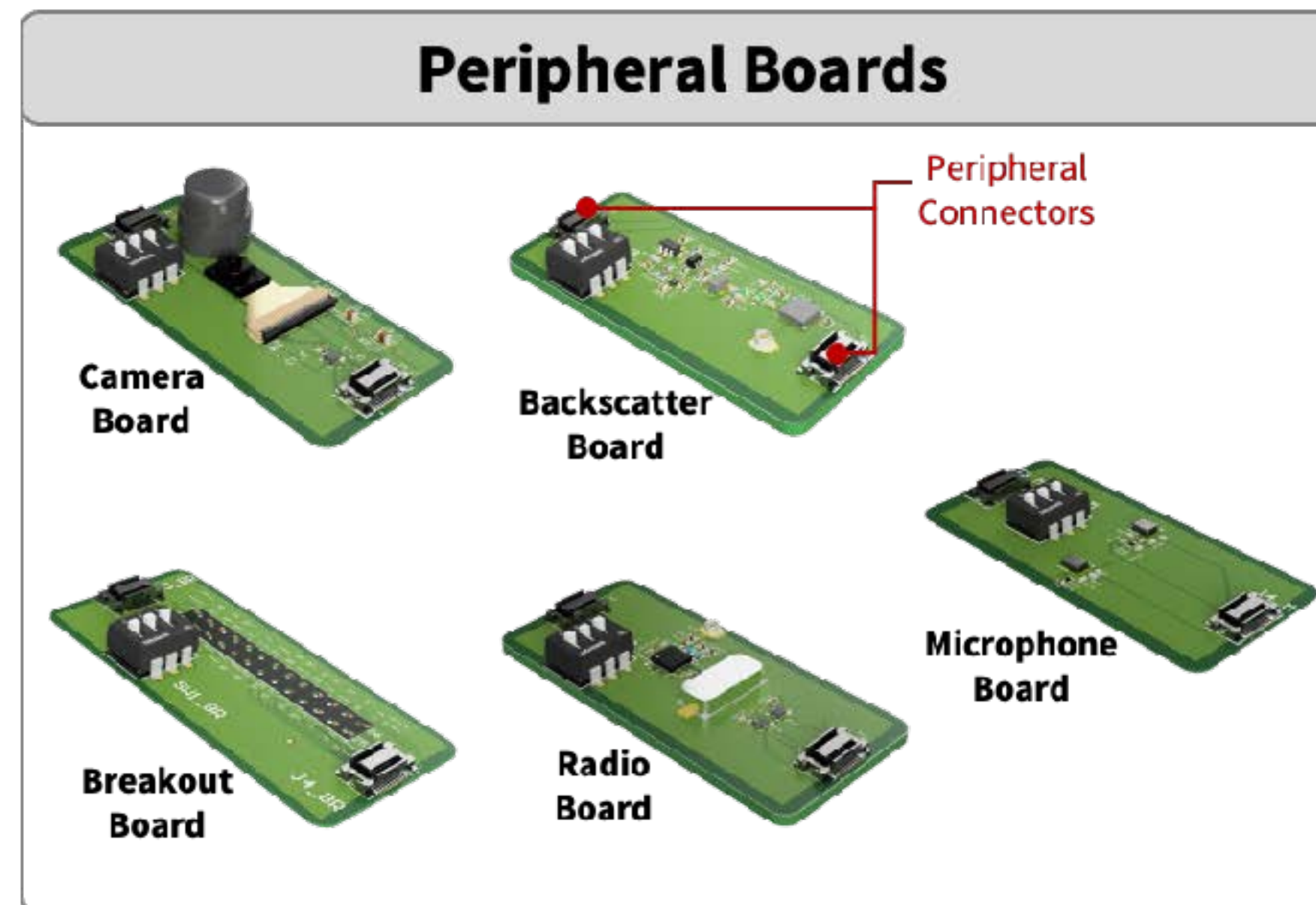
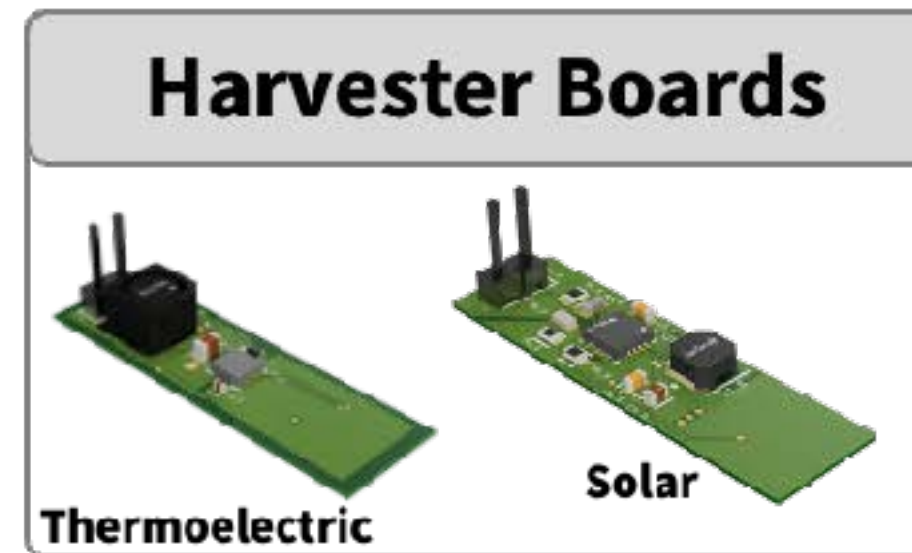
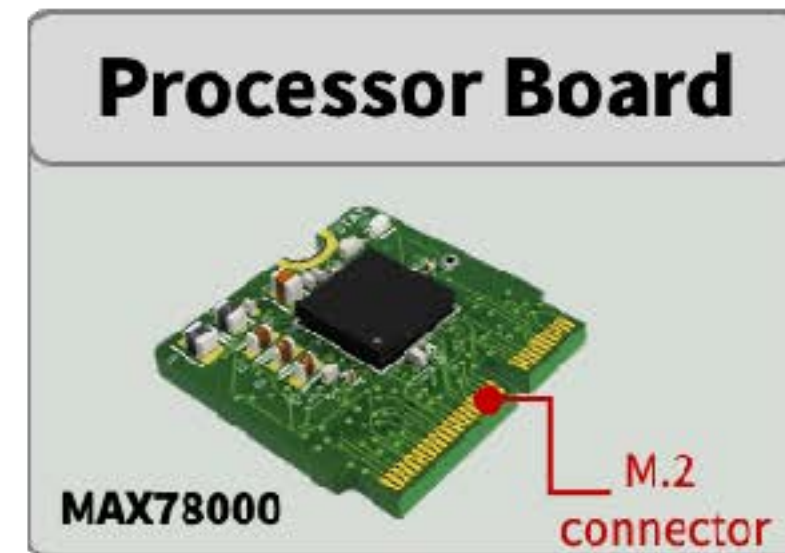
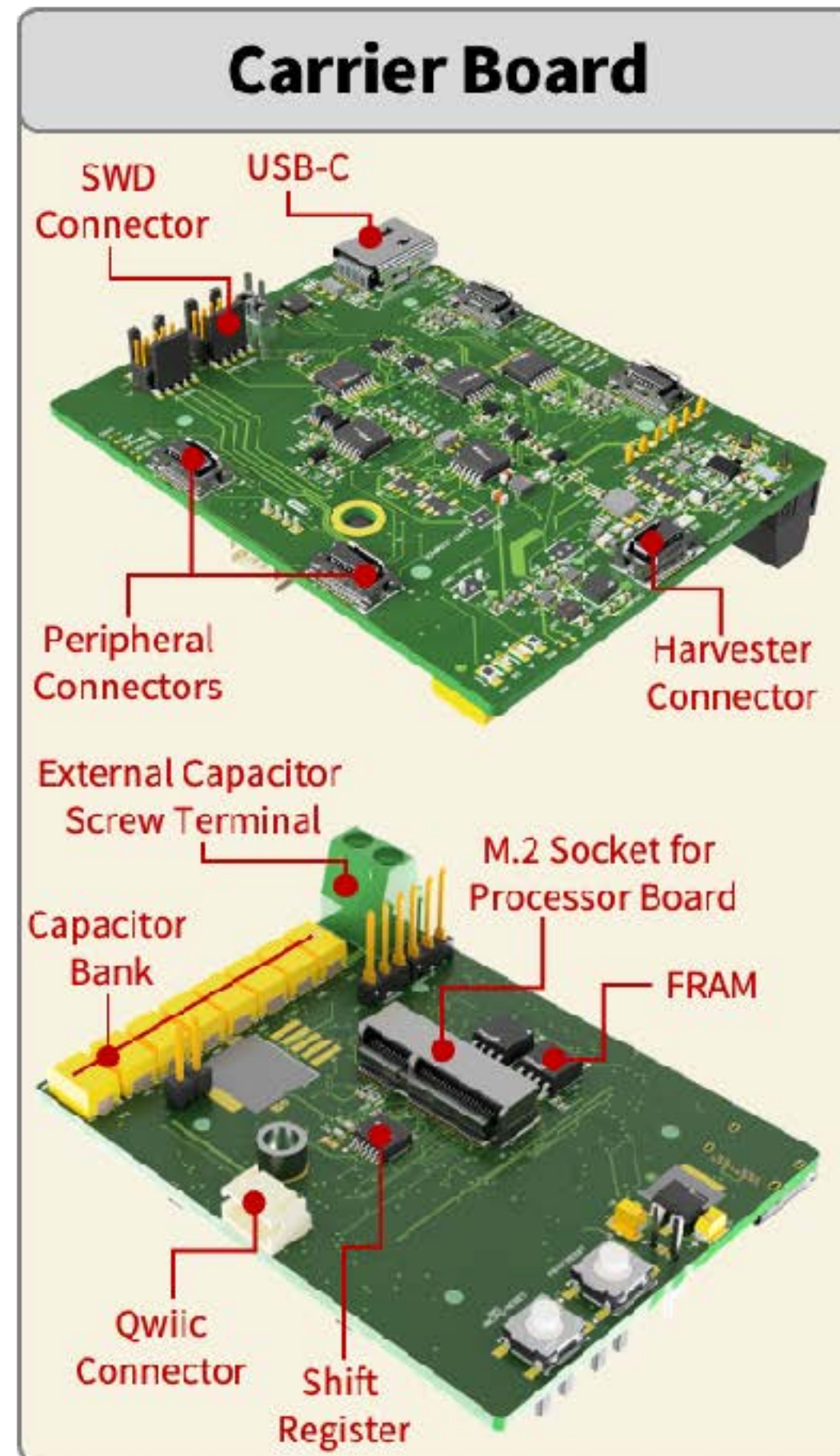
...so they reboot multiple times a second



piece together execution times across power failures...

Failure Resilient Architectures and Hardware

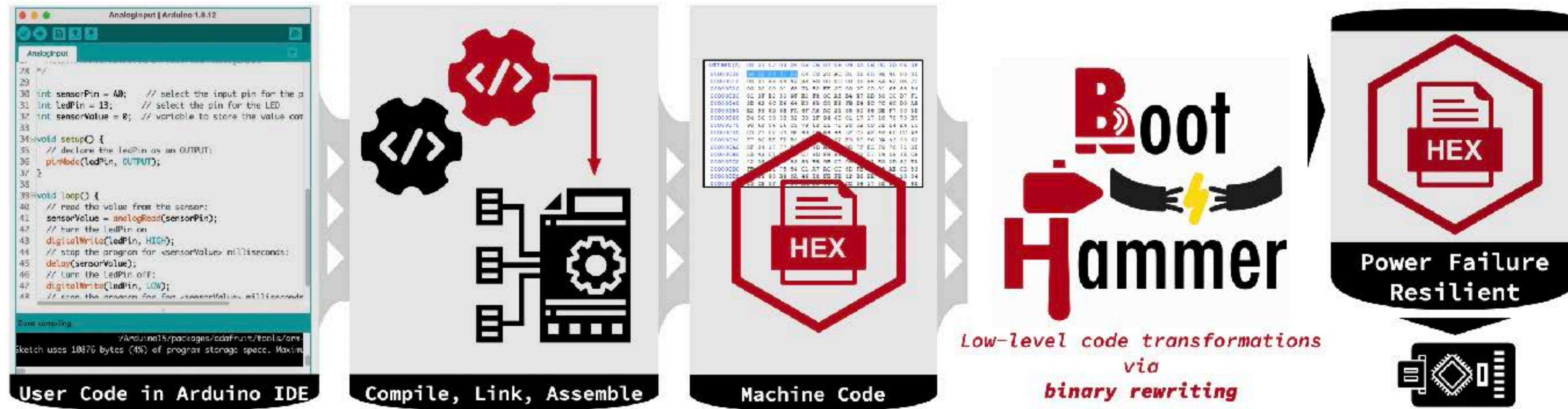
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Novice Friendly Intermittent Computing

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Accessible energy harvesting and battery-free embedded systems via integration with Arduino and Microsoft Makecode



Societal and Scientific Impact

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Work with Tribes on Sustainable Environmental Sensing



Hawaii Efforts



Micro:bits in STEM classes: Mini activities with sensor data



research

DOI:10.1145/3624718

Batteryless, energy-harvesting systems could reshape the Internet of Things into a more sustainable societal infrastructure.

BY SAAD AHMED, BASHIMA ISLAM, KASIM SINAN YILDIRIM, MARCO ZIMMERLING, PRZEMYSŁAW PAWEŁCZAK, MUHAMMAD HAMAD ALIZAI, BRANDON LUCIA, LUCA MOTTOLA, JACOB SORBER, AND JOSIAH HESTER

The Internet of Batteryless Things

IMAGINE USING A health bracelet that tracks your blood pressure and glucose level that you do not have to charge for the next 20 years. Imagine sensors attached to honeybees helping us understand how they interact with their environment or bio-absorbable pacemakers controlling heart rate for 6–8 months after surgery. Whether submillimeter-scale “smart dust,”²⁵ forgettable wearables, or tiny chip-scale satellites, the devices at the heart of the future of the Internet of Things (IoT) will be invisible, intelligent, long-lived, and maintenance-free. Despite significant progress over the last two decades, one obstacle stands in the

way of realizing next-generation IoT devices: *the battery*.

Batteries provide the convenience of a reliable energy supply but create a host of problems. Batteries limit device lifetime and yield high maintenance costs. As device size has continued to scale down, battery density scaling has not kept pace. As IoT device applications demand more computational capabilities, energy limits lifetime to weeks or months. Even rechargeable batteries have a limited lifetime, wearing out after 300–500 charge cycles.

As we move toward a future with trillions of IoT devices,^a replacing trillions of dead batteries and devices will be both prohibitively expensive and irresponsible. A future IoT with trillions of new battery-powered devices would create an environmental catastrophe.

Most discarded batteries end up in landfills—only 5% are recycled. Discarded batteries release toxic fumes into the air and disperse chemicals in the soil as they break down. When batteries are recycled, the process releases contaminants into waterways.⁷

Batteryless devices and intermittent executions. During the last decade, and building on work from the decades prior, research pushed toward a new kind of system that is pervasively deployed,

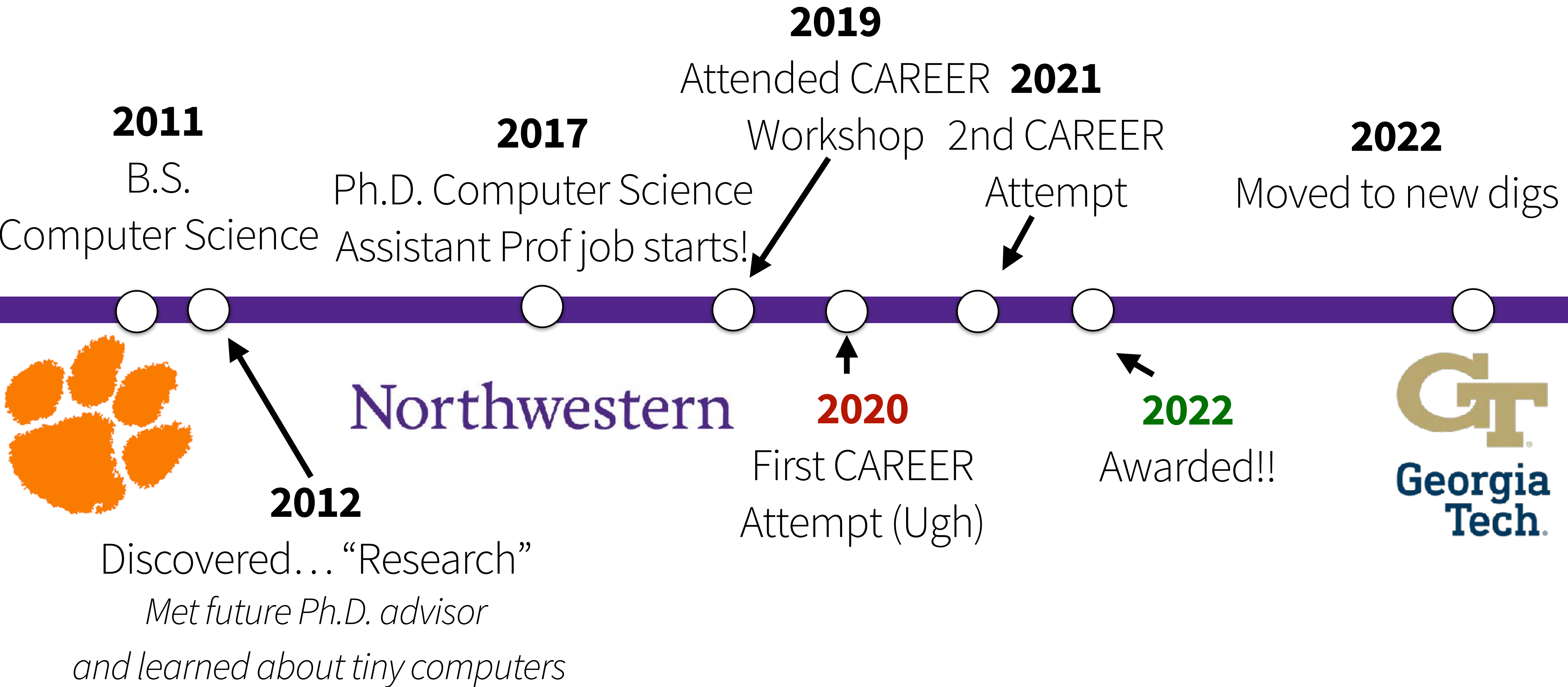
a <https://bit.ly/491LSNE>.

» key insights

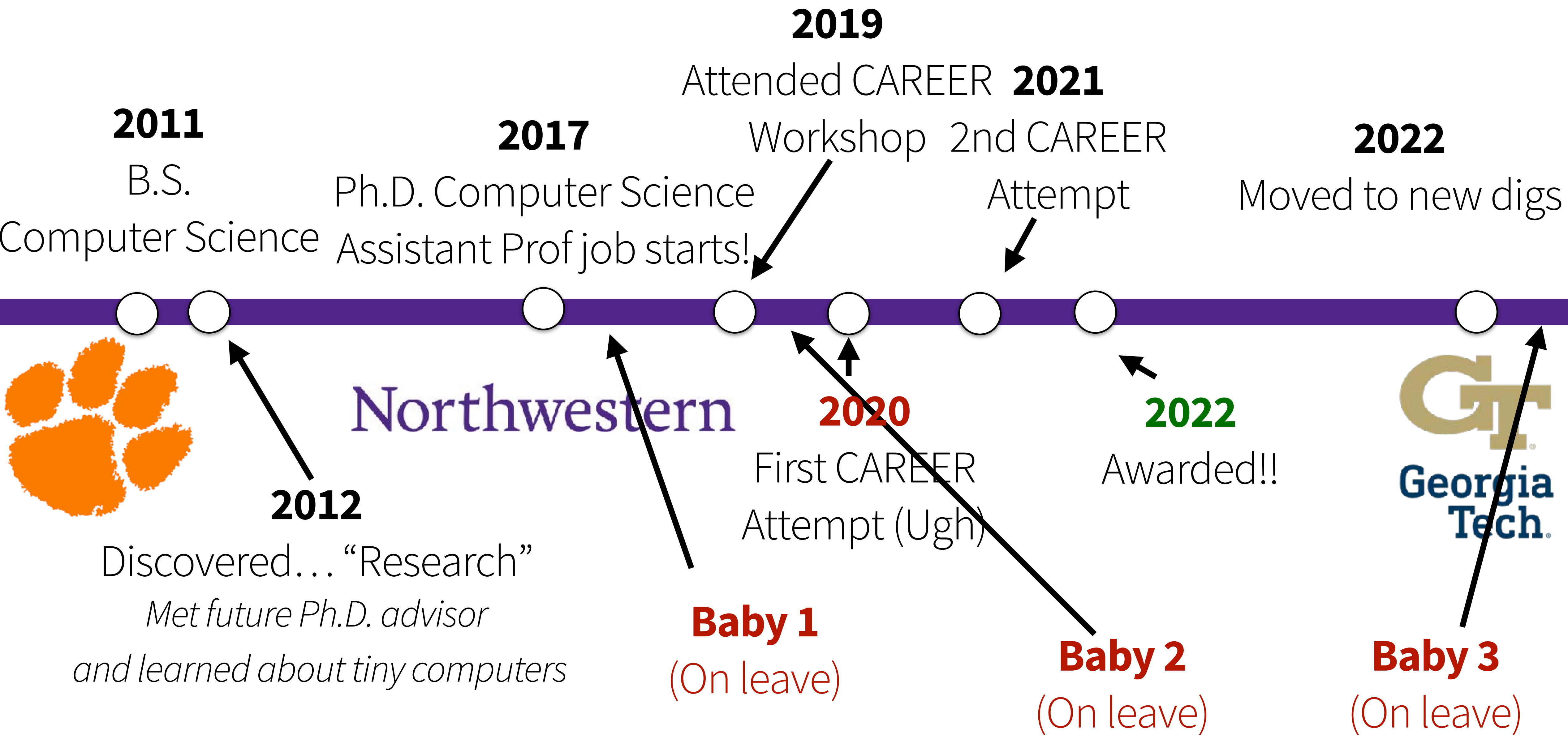
- As we move toward a future with trillions of IoT devices, replacing batteries will be both prohibitively expensive and irresponsible.
- Over the past decade, research produced new energy-efficient programming languages, compilers, runtime systems, and architectural designs that enable real-world applications of batteryless devices.
- Albeit existing work laid a foundation for batteryless, energy-harvesting computing, the field is arguably at a stage where a much bigger leap is needed for this technology to gain widespread adoption. We discuss six fundamental directions we maintain to be crucial for the field to thrive.

IMAGE BY ANDREJ BOBYL ASSOCIATES, USING SHUTTERSTOCK

Timeline



Timeline



Philosophy

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Philosophy

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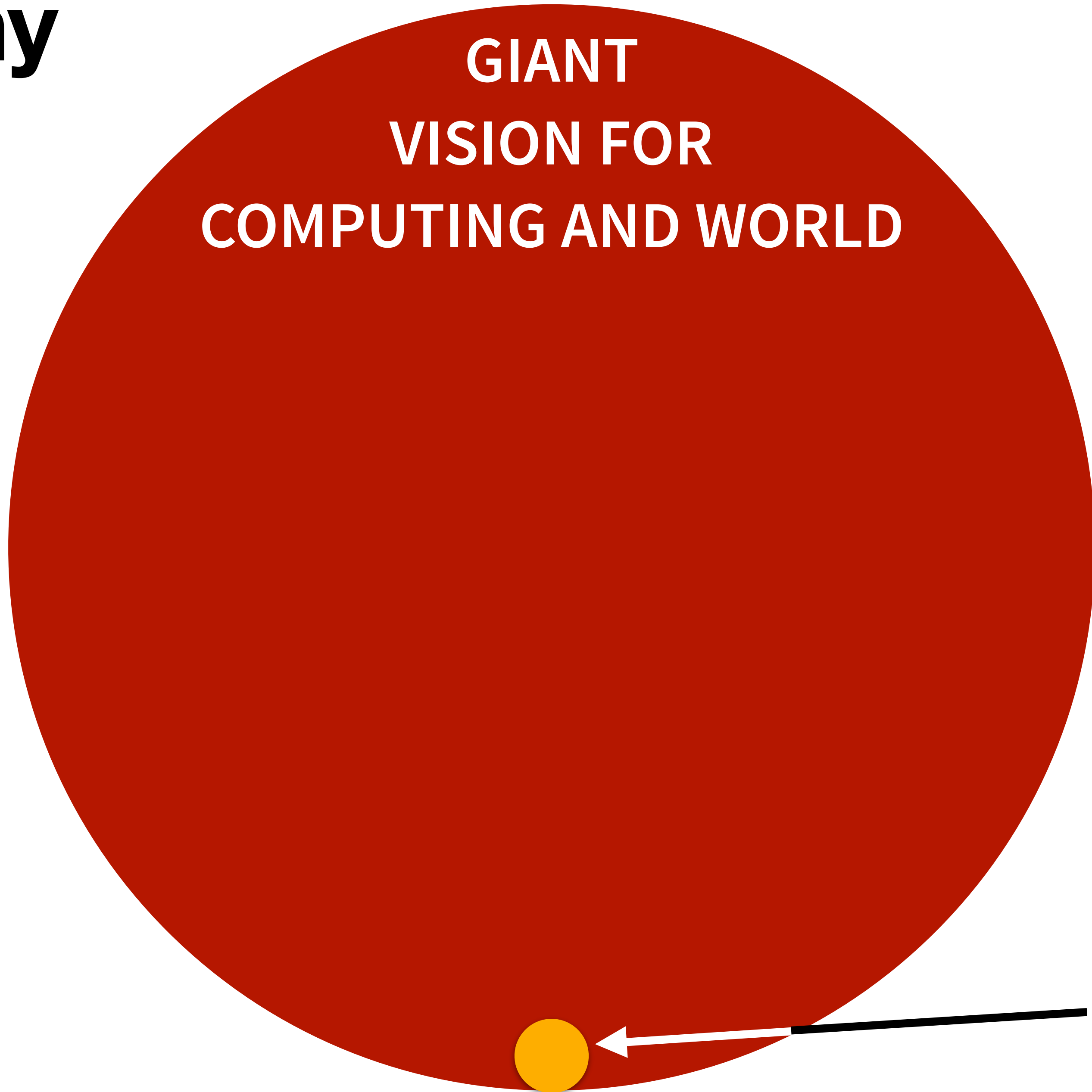
GIANT
VISION FOR
COMPUTING AND WORLD

Philosophy

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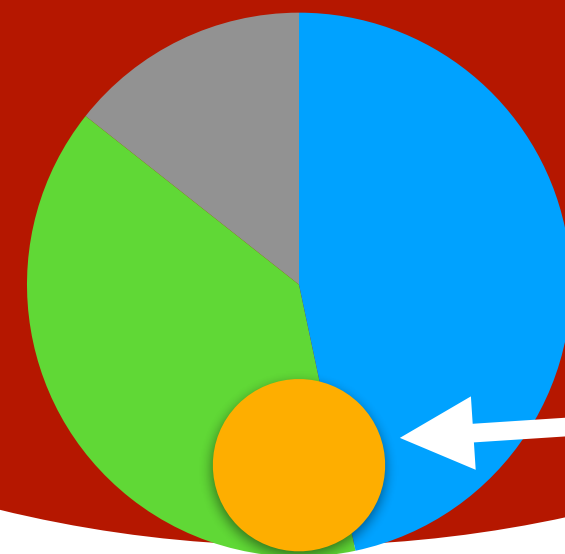
My Ph.D.
(Not to scale)



Philosophy

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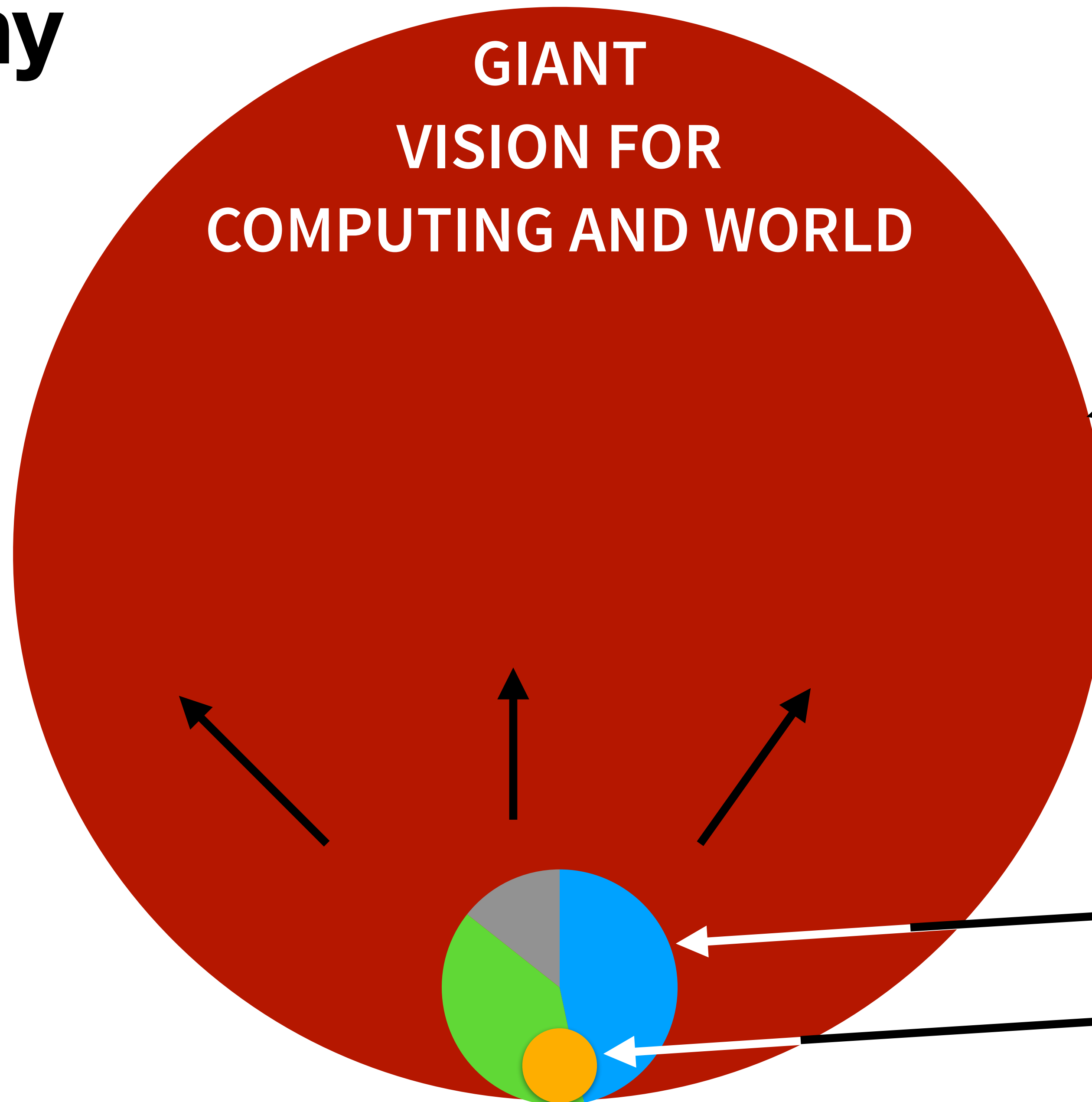


My "CAREER"
My Ph.D.

(Not to scale)

Philosophy

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Philosophy

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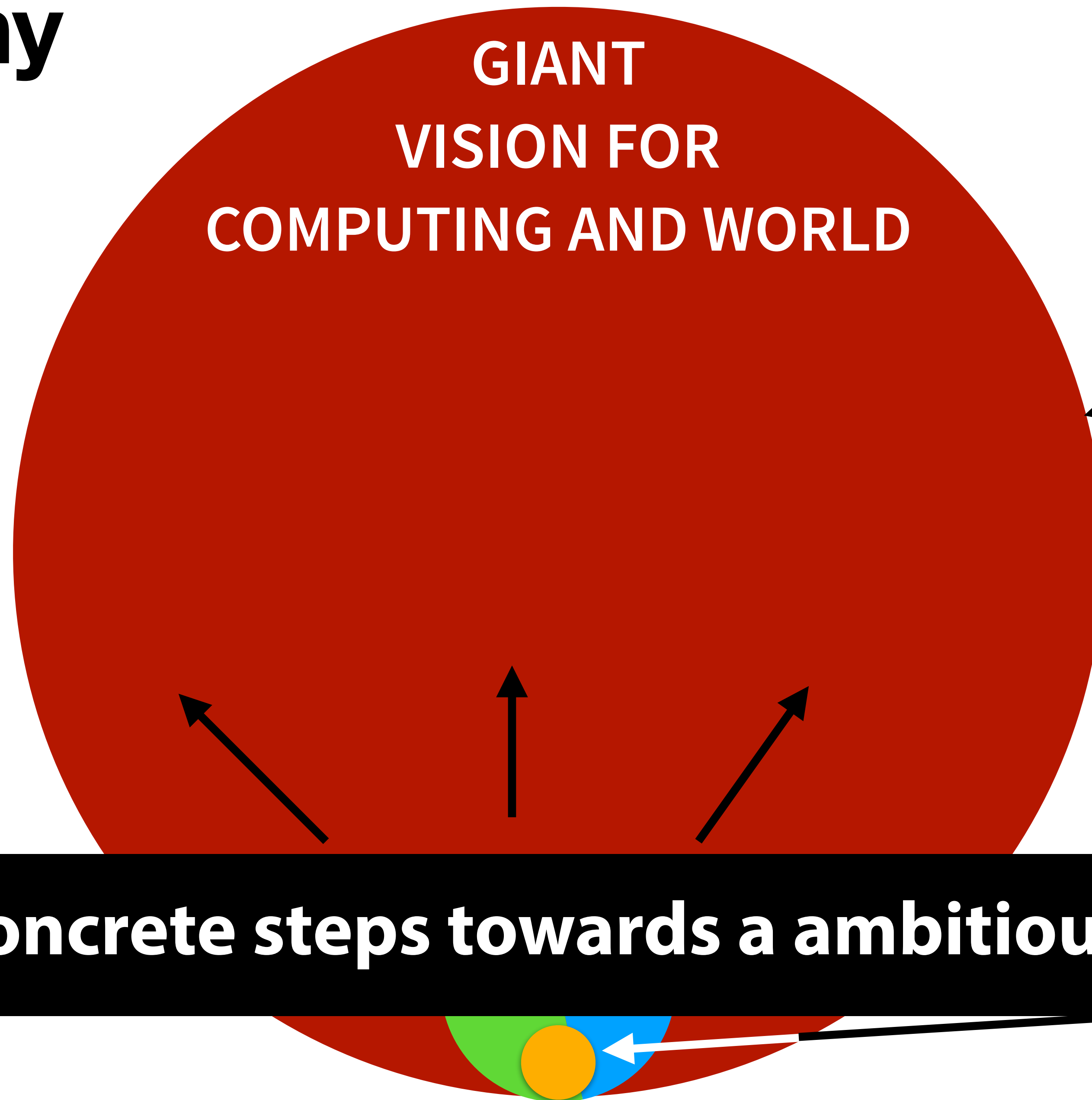
GIANT
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My Career :)

I hope!

Show concrete steps towards a ambitious vision!

(Not to scale)



Philosophy (My Ideal! – *you may be different*)

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- Give a **vision of the future** that is exciting, and show the first few steps.
- This is your chance to really dig deep on what you want to do and maybe even... **Who you are???**
- Write out your big vision– with the initial small reasonably clear steps. The steps **do not have to be** earth shattering, just needs to be clear.
- Help reviewers and PDs find **something** they can champion.
- It really helps to be earnest. Play to **your strengths**.

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• It really helps to be correct. Play to your strengths.

This is just me! How you arrive may be different.

My CAREER Guided Tour

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Short motivator and “the point”!

Battery-free embedded systems offer a transformative and ecologically sustainable approach for building the next trillion computing devices. Yet, sophisticated applications still seem out of reach. System designers lack the hardware platforms, efficient runtime systems, and focused tools to build capable, data-intensive, reactive, and reliable applications on these devices. This proposal seeks to address these shortcomings.

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This proposal seeks to fill the gap in hardware platforms, runtime systems, and tools for practical, dynamic, and capable applications on intermittently powered embedded systems.

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Summarize the whole proposal in box

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Define the problem of this proposal

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My CAREER Guided Tour

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Describe the approach, merits, impact!

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The first page (of any proposal) does a LOT of work!

My CAREER Guided Tour

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Gave binding **themes** of the work.
Conceptual **answers** to the challenge.

1. **Leverage hardware heterogeneity and weave its benefits across the system stack.** We can overcome the energy-per-computation barrier keeping us from capable applications by using low-power accelerators and FPGAs. However, the intermittent systems support for this is nascent at best.
2. **Embrace energy-aware adaptation, dynamism, and approximation.** Energy harvesting is inherently dynamic; the applications that run off this energy should be scaling operations based on energy available instead of just giving up. We must create scalable and efficient runtime systems that work no matter the energy situation.
3. **Equip developers with a new generation of sophisticated tools.** Building applications that can scale computation across intermittent power failures, heterogeneous hardware, and dynamic energy are challenging. We must develop tools that give insights into energy generation and usage and show the many paths an application can take caused by dynamic energy availability.

1.1 Vision, Goals and Technical Approach

This proposal advocates for a future Internet-of-Things where the predicted trillion devices are battery-free, interact seamlessly with a user, sense, and infer large amounts of data in real-time, all to inform countless applications across societally essential domains. In this future, battery-free devices will be easy to program, straightforward to test and deploy, with scalable and capable hardware platforms and systems. Programmers will have the tools to manage the volatility of energy harvesting and power failures and build resilient code for complex and practical applications that combine sensing, machine learning, and communication. Developers will finally have confidence in a deployed battery-free embedded system. This proposal outlines three conceptual and practical answers to the shortfalls previously identified that can realize this vision:

1. **Leverage hardware heterogeneity and weave its benefits across the system stack.** We can overcome the energy-per-computation barrier keeping us from capable applications by using low-power accelerators and FPGAs. However, the intermittent systems support for this is nascent at best.
2. **Embrace energy-aware adaptation, dynamism, and approximation.** Energy harvesting is inherently dynamic; the applications that run off this energy should be scaling operations based on energy available instead of just giving up. We must create scalable and efficient runtime systems that work no matter the energy situation.
3. **Equip developers with a new generation of sophisticated tools.** Building applications that can scale computation across intermittent power failures, heterogeneous hardware, and dynamic energy are challenging. We must develop tools that give insights into energy generation and usage and show the many paths an application can take caused by dynamic energy availability.

This proposal considers two broad classes of devices that have emerged as the dominant future for intermittent computing. *Invisible devices* are those that sense and process data without interaction from humans, such as in large-scale infrastructure monitoring, sensor networks, wildlife surveillance, etc. These devices must meet sampling deadlines and do sophisticated calculations to enable critical applications. Invisible devices must balance the need for seamless and continuous data and inference with the reality of dynamic energy harvesting. *Interactive devices* are those that respond or interact with humans for an application purpose, for example, health wearables, gaming devices, and interactive displays. Because of the unpredictability of harvested power, these devices are rarely deployed, and represent a critical gap in the research, as these *reactive, interactive, and screen-focused* systems are a significant portion of current and anticipated intelligent systems. Interactive devices are challenging as they must be reactive to user input and requests via the screen, vibration, or otherwise, and require rich compute and hardware resources.

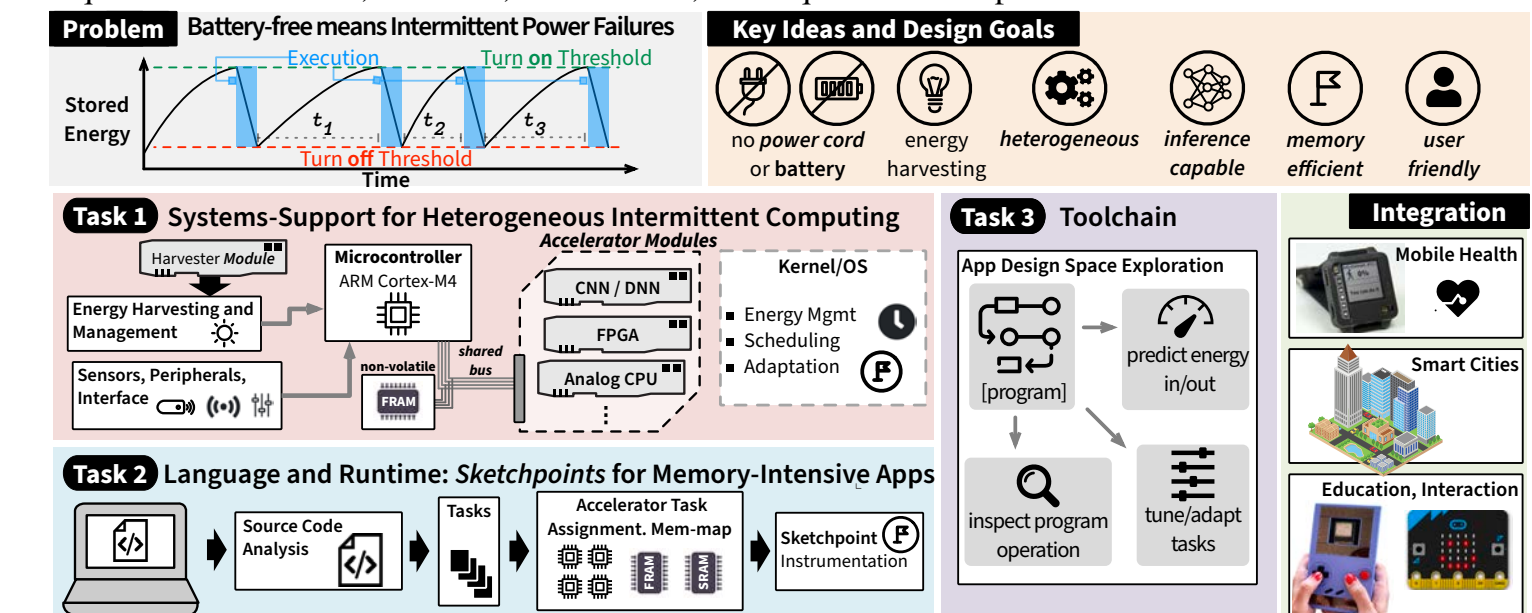


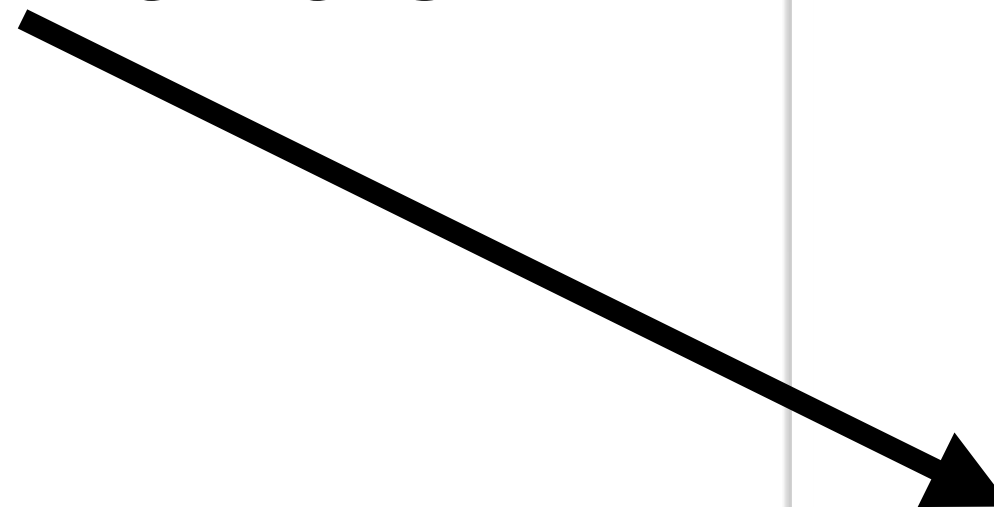
Figure 1: The BFree Ecosystem for Battery-free, Energy Harvesting, Failure Resilient Embedded Computing: a holistic approach to prototyping, designing, testing, programming, and deploying battery-free smart devices.

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Stupidly complex figure 😅

The hope is to tie it all together for reviewers.



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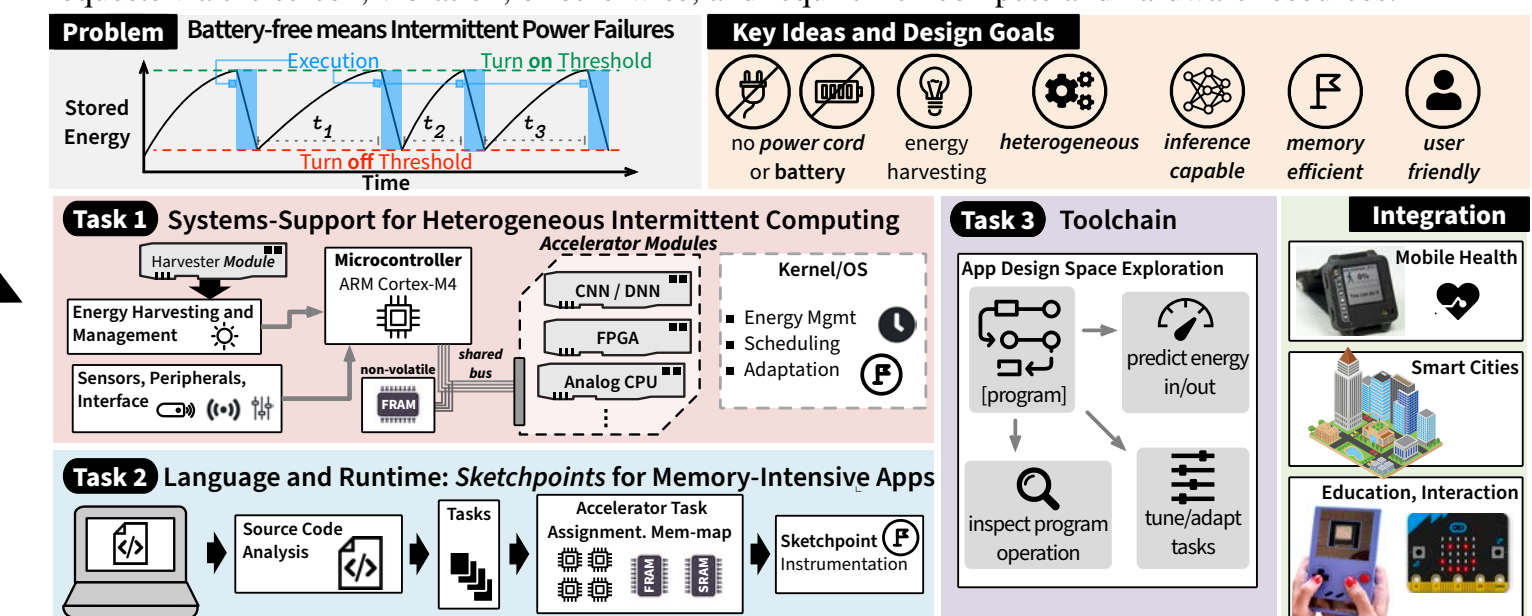


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Finally get to the **essential** research **tasks**
For me... These are each a **series** of papers.



These devices have shared challenges; overcoming power failures to meet deadlines, efficient checkpoint and restore operation, high programmability, rapid prototyping and testing, and seamless adaptation and scalability. Current approaches do not provide graceful ways to adapt the output to changes in the energy environment, are limited in computing capability, and are constrained by the overhead of saving and restoring state across power failures.

The work in this proposal revolves around the development of the **BFree Ecosystem**. An overview of our approach, including tasks and key ideas, is shown in Figure 1. BFree is a cross-stack approach to systems building that re-imagines core concepts in the context of intermittent computing. Each research task in isolation offers many rich problems to explore; by pushing on all areas to map out as much of the space as possible, we can identify new grand challenge research problems and killer applications and better equip the research community. The work is wide-ranging and involves building real systems and tools—including software and hardware artifacts—and evaluating them with real data, deployments, and users. BFree will lay a foundation for intermittently powered smart devices to be built and deployed by novices and experts alike in countless applications in the future Internet of Things. We engage in the following interwoven research tasks

Task 1: Hardware and Systems-Support for Heterogeneity. Accelerators are ubiquitous in high-performance mobile computing. Intermittent computing has not yet integrated specialized and general purpose hardware in a single platform due to the challenges stemming from heterogeneity and mixed memory volatility. This thrust builds a reconfigurable, modular, and deployment-ready hardware platform that embraces multiple computing forms—microcontroller (MCU), convolutional neural network accelerator (CNNA), FPGA. The key design principles are (i) embrace dynamism in energy availability, from nano-watts to 100s of milli-watts, (ii) enable rapid reconfiguration at design and runtime, and (iii) provide low-level systems support for separating compute tasks across computational elements.

Task 2: Language and Runtime Support: Sketchpoints and High-Level Programming. Checkpoint costs for memory-intensive applications often exceed the energy budget. This makes it challenging to build data and memory-intensive or inference-focused applications with a high level of sophistication (i.e., millions of weights in a CNN versus thousands). The task proposes "sketchpoints" and hierarchical checkpointing, both means of summarizing the state of a system in a checkpoint instead of saving a differential or the entire volatile state to non-volatile memory. This task builds on these approaches to create efficient inference applications and transpilers for high-level programming languages for battery-free devices so that novices can program in scripting languages like Python, JavaScript, and Blocks (like Scratch [68] and Makecode [67]).

Task 3: Developer Tools and Energy Insights. Heterogeneity of the BFree hardware platform causes headaches in understanding where energy is being used and which computing elements are responsible for program tasks. Understanding how an application will change (i.e., how accuracy might decrease) as energy decreases is critical to careful design. This task builds tools for the simulation and emulation of scalable intermittent computing applications. We develop a simulation tool that helps developers explore the energy-driven design space and fine-tune intermittent applications as they write their code.

Integration–Deployment in the Real World. The research proposal tasks, education, and outreach activities are all integrated via real-world deployment and testing with the SAGE project at Argonne National Lab to deploy smart cities and remote conservation applications, and with with clinicians in Northwestern's Medical School and to deploy mobile health devices (smart face masks, fitness trackers) .

Intellectual Merit. The proposed work is the first effort to tackle the systems-support and scalability research challenges in integrating heterogeneity within intermittent computing. The core of the work is on speeding up computation on energy and resource-constrained devices, a core challenge in computing. We apply these techniques to an important class of devices (batteryless, energy harvesting) to enhance applicability. The project will: (i) develop hardware platforms with diverse computing elements in a modular form factor, with runtime level abstractions to seamlessly move computation to the most efficient placements; (ii) evolve efficient checkpointing schemes for memory-intensive applications and high-level programming models; (iii) democratize access to intermittent computing with energy-aware tools for supercharging development.

My CAREER Guided Tour

KA MOAMOA

Rephrase and go **deep** into the problem
Reviewers are not in **your sub-area!**

Break down the main **challenges...**

2 Background

Intermittent computing is the fundamental model of computation underlying battery-free embedded systems and the primary area of this project. Relying on volatile harvested energy makes computation, communication, and sensing very likely to be *intermittent*. Figure 2 shows this intermittent operation, where power failures intermingle with moments of operation, and the runtime must string together fragments of execution to meet application goals. Power failures become a frequent occurrence. Recovering gracefully and efficiently from those power failures has been the theme for intermittent computing research [38, 57] since 2011.

Intermittent computing has gone from a niche exploration in 2011 to an area with significant academic and industrial research efforts. The publication of the MementOS [77] paper at ASPLOS 2011 described a first checkpointing approach for active RFIDs that intermittently operate because of the multi-path and attenuation of RFID reader energy. Since then, the intermittent computing community has shown vibrant growth, with multiple labs worldwide conducting high-profile work. These labs have deployed battery-free devices to safeguard national monuments [1], put them into space [58], and in homes [47], and in the PI's work, built a Battery-free Nintendo Game Boy. The last project was the first demonstration of complete system virtualization with intermittent computing (covered by the BBC, Washington Post, CNET, and others) [20].

Industry efforts have emerged in the past couple of years. Arm's Triffid project [70] is building low-power microprocessors meant for battery-free operation, noting that "The greatest challenge the Internet of things faces is how those 'things' will be powered." Nokia Bell Labs' has initiated efforts on wearable computing angling towards battery-free wearables [69]. Most recently, Communications of the ACM did a feature on the area, marking the first time the area showed up in the flagship publication of computing, where PI Hester (and colleague Brandon Lucia) were heavily quoted on intermittent computing for a battery-free IoT [82].

Since MementOS, researchers have addressed the *intermittent computing* challenge by designing methods to ensure forward progress and maintain data consistency across repeated power failures. Software-based solutions have tried to mitigate the shortcomings of intermittent operation either by instrumenting programs with checkpoints [8, 77], or by rewriting applications using task-based programming models [40, 60, 96]. Hardware and platform approaches have focused on reducing the cost of checkpointing [42], managing energy more efficiently to reduce power failures, and increase event detection [17, 35, 36], and getting a rough estimation of time elapsed between power failures [41, 76]. Despite progress, inference-focused, memory-intensive, general-purpose intermittent computing is still out of reach because of three challenges.

C1: Low Performance and Scalability. Besides the PI's recent work, every intermittent platform has used the Texas Instruments 16-bit MSP430 FRAM series [91], which has 256KB of FRAM, 8KB of SRAM, and a processor that can barely reach 16MHz. Because of this low capability, even state-of-the-art approaches for machine learning on intermittent power [29, 46, 69] have only demonstrated predictions using 1000s of weights for simplistic applications like gesture identification or presence detection. While innovative techniques for multi-exit inference [46, 95] and weight pruning [69] have extended the usefulness of 16-bit platforms, the field needs a drastically expanded capability to support future applications. 32-bit MCUs and the use of heterogeneous compute elements like CNN accelerators and FPGAs are promising. Still, integration and system support are utterly lacking because of the research challenges of sharing compute tasks across heterogeneous resources in the face of intermittent power and dynamic energy.

C2: Handling Memory-intensive Programs. Large amounts of memory are moved back and forth to peripherals or across computing elements in many critical applications. Data-intensive health sensing, video/audio-based wildlife surveillance, and gaming are three areas PI Hester works that exhibit memory-intensive operation. As heterogeneity increases, so too will the demands on memory efficiency. Naively

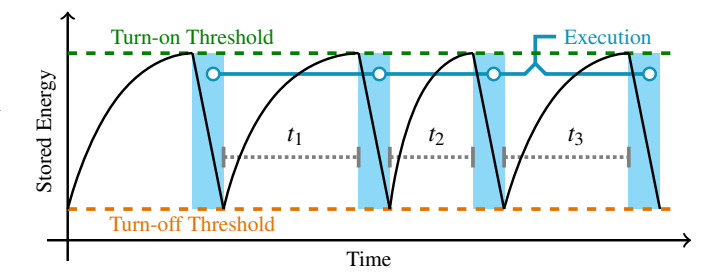


Figure 2: Battery-free energy harvesting computers fail intermittently. Research problems come from preserving state of execution across power failures.

My CAREER Guided Tour

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Now we really get into the meat of the work
My approach was **most mature** research tasks first
We had preliminary data for T1.

Made it easier to write about!



checkpointing the entire system state is impractical or infeasible when memory are distributed across multiple accelerators. Recovery of large state is slow and tedious with per component variable latency. The new generation of inference-heavy and heterogeneous intermittent computing requires a rethinking of how we design and implement checkpoint and restore operations.

C3: Lack of Developer Accessibility and Support. The few tools that exist for intermittent computing are inadequate for heterogeneous platforms, inference applications, and understanding energy-aware adaptation and scalability. Adaptation or approximation has emerged as a reasonable method to adjust operation (for example, accuracy) based on the energy available. However, no tools exist that help the developer explore this design space and tradeoffs. No tools exist for understanding the tradeoffs between hosting computation on the MCU versus the FPGA and the memory impact of that decision. In essence, the design and tradeoff space for intermittent computing on heterogeneous platforms is immense. Developers need an atlas and new tools for navigating this process.

These challenges represent a tremendous opportunity for research into system support for intermittent computing on heterogeneous platforms. The PI is a leader in intermittent computing, especially real-world applications and sensing systems. The PI has led significant work to make intermittent systems reliable and consistent [40, 50], building novel hardware [18, 20, 36, 41], programming languages [49, 96] and tools [27, 34] to speed up development and deployment of battery-free embedded computers. These works appeared in ACM SenSys (x7), ACM ASPLOS(x2), and ACM UbiComp/IMWUT(x3), including a Best Paper Award and Best Paper Nominee at SenSys. The PI is active in leadership in the field as Steering Committee Member and former Program Chair for ENSsys, the premier workshop for Energy Harvesting systems co-located with ACM SenSys since 2013. Because of this background and prior work, PI Hester is uniquely positioned to carry out the proposed work.

3 Research Plan

We propose a new ecosystem for intermittent computing, *BFree*, to address the challenges inherent in running high-performance and scalable applications on tiny battery-free devices. The *key idea* of *BFree* is to embrace the *dynamism* of energy harvesting and *heterogeneity of platform* across every layer of the system stack. This plan describes the systems research tasks from, hardware, software, tools and integration.

3.1 T1: Hardware and Systems-Support for Heterogeneity in Intermittent Computing

energy harvesting availability and power failures. Energy harvesters have a huge dynamic power output range. A solar panel the size of a credit card, can output from 100s of microamperes in deep shade to a quarter of an ampere in bright sunlight. This is a difference of 3-4 orders of magnitude; this solar panel could power a streaming image recognition task using a neural network on the upper end of this range. On the lower end, the solar panel could barely power motion detection. Other types of energy harvesters, like RFID, microbial, thermal, have irregular ranges but can support high peak power if conditions are right. In this task, we build a platform to take advantage of this dynamism: a reconfigurable, modular, heterogeneous hardware platform that will tackle research problems in battery-free devices to enable both high performance and ultra scalable intermittent computing for novel applications. Task 1 in Figure 1 shows the high level overview of the platform and Figure 4 shows the proposed layout.

Why Heterogeneity for Intermittent Computing? Intermittent computing can leverage the dynamic range of energy harvesters with heterogeneity. Special-purpose computing components like accelerators and FPGAs have recently become low power enough to be feasible in small and energy harvesting devices. These com-

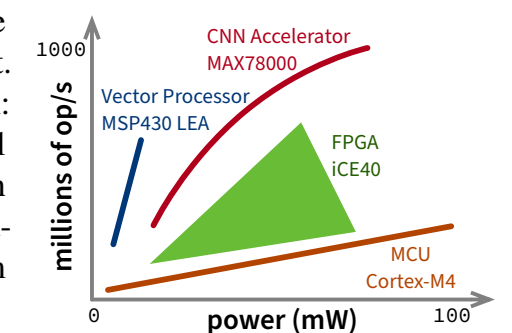


Figure 3: Heterogeneous intermittent computing opens up high performance applications and larger dynamic range.

My CAREER Guided Tour

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Now we really get into the meat of the work
My approach was **most mature** research tasks first
We had preliminary data for T1.

Made it easier to write about!



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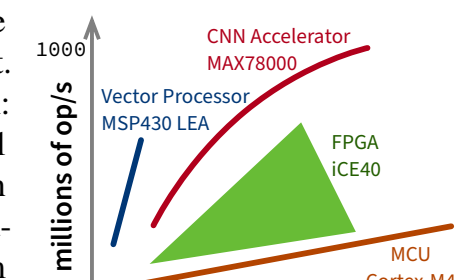
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Entertain and engage reviewer! Show “neat” tricks.

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Now go into “research paper” mode...
Give detailed prior art, suggest ideas...
Provide literature and reasoning for justification.

ponents provide significant speedup for narrow, yet, critical tasks, compared to a general-purpose CPU executing that task. As machine learning and data-driven computing become the essential tasks in many wearables and wireless sensor network deployments, these specialized accelerators become invaluable for providing high application-specific performance in a small power budget. Significantly, these specialized accelerators increase the ceiling of what can be done on intermittent power. Figure 3 shows this tradeoff for off-the-shelf accelerators which have higher performance per Watt in comparison to existing intermittent computing platforms. Of course, this does not come without a cost.

What is the Ideal? Consider a battery-free device inserted in a face mask predict breathing, respiration, coughs, and activity of the wearer on-the-fly, powered by the breathing and motion of the wearer. This application is infeasible with current 16-bit, slow, general-purpose processors used in intermittent computing. An ideal situation has a pipeline of accelerators that processes and draws inferences from the data. If energy is low, the system automatically degrades performance to meet deadlines. It may even move an inference task from a more accurate (but higher power) accelerator to a less accurate but fast algorithm running on the microcontroller. For the high energy state, an ultra-low-power FPGA (like the Lattice iCE40 [53]) functions as a bandpass, signal separation, and feature extraction steaming processor from the motion sensors. These features are fed to a Convolutional Neural Network (CNN) accelerator (like the Maxim MAX78000 [65] which supports two million weights), which predicts the wearer's activity. The microcontroller shuttles data around these accelerators and maintains memory consistency and progress despite power failures by careful checkpointing. The microcontroller disables all accelerators in low energy and runs a simple, low accuracy algorithm. This algorithm differentiates between "active" and "not active," whereas the high power setup with FPGA and CNNA could distinguish specific activities like running, walking, coughing. Each of these heterogeneous computing components provide a spectrum of ways to scale the power draw by giving up latency, accuracy, or computation complexity.

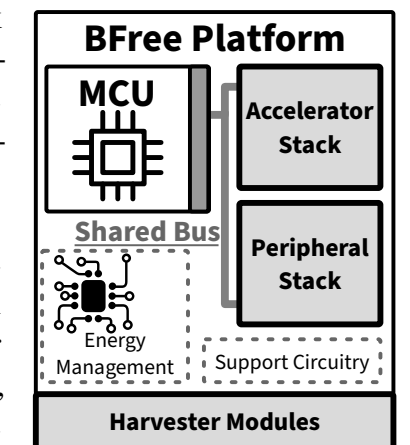


Figure 4: Envisioned modular heterogeneous platform.

To move beyond the monolithic 16-bit microcontroller approach to intermittent computing, we must embrace heterogeneity and overcome the numerous difficulties this entails. The systems' *challenges* lie in the intersection of intermittent power, dynamic energy, and heterogeneity. The systems' *impacts* lie in the increased performance and applicability for intermittent computing. **The challenges include:**

1. **Navigating the Architectural Design Space of Heterogeneity.** The first challenge is a design tradeoff space one. Current applications range from simple temperature sensing to complex inference on vision tasks. How can one experimental hardware platform support both of these incredibly different domains? What are the hardware-enabled breakpoints, accelerators, and inference problems that must be supported? What practical concerns (i.e., obsolescence) might stymie research?
2. **Scaling / Degrading Tasks in the Face of Dynamic Energy.** The fundamental question is: where, when, and at what quality should compute tasks happen? This is complicated by intermittent and often unpredictable failures. Figure 3 shows the spectrum of computational load to energy across different devices. The operating system must leverage signals and information from the programmer, environment, and execution to optimize compute and memory placement across the heterogeneous devices available for the best performance. Artful hardware and systems support is needed to schedule these tasks and enable seamless execution across the heterogeneity of hardware and power failures.

When we tackle these problems, we are confronting old systems problems in a new context: old problems like cache coherency and consistency (i.e., memory consistency across computing components and shared memories on a device), in a new framing and challenging space with dynamic power, frequent failure, and constrained resources. Leveraging insights from traditional systems are not enough, we must come up with new systems and build real-world demonstration platforms from the ground up to test ideas.

My CAREER Guided Tour

KA MOAMOA

Weave in any **previous publications** you have!
Especially if they lead or support your idea.

I led with this Task, since had **prior work!**

Makes it simpler to be **concrete** with reviewers.

3.1.1 Prior Work

The most relevant prior work to this task is Capybara by Colin et al. [17], Dynamic Energy Burst Scaling (DEBS) by Gomez et al. [30], and Flicker [36] by the PI (shown along with other platforms made by the PI in Figure 5). While hardware platforms for battery-powered embedded systems go back to Telos [74] and MicaZ "motes," Flicker and Capybara were the first platforms to enable general-purpose intermittent computing. Both approaches use programmable capacitor arrays to match computational tasks to available energy and stave off power failures. Flicker enables rapid prototyping of battery-free intermittent computing devices such that designers can rapidly configure new devices for applications in environmental monitoring, activity detection by using a novel interconnect and modular design [35, 36]. DEBS is an approach to scale execution from 100s of microwatts to tens of milliwatts at the power converter level. Other battery-free platforms [18, 35, 71, 83, 88, 100], focus on enhancing a particular part of the system stack, like timekeeping or energy storage, or sped up a particular application, instead of providing a general platform. All works referenced in this section target older 16-bit microcontrollers (MSP430s), losing out on the potential performance increases of modern 32-bit ARM M-series MCUs and accelerators. None of these approaches consider scaling tasks across different computing modalities like accelerators, FPGAs, and MCUs. To date, no general-purpose heterogeneous platform for battery-free devices has been developed. A recent viewpoint paper at HotMobile [80], and architecture letter [21], highlighted the possibility and promise of heterogeneity for deep neural net acceleration, but so far no general hardware platforms yet exist embracing these concepts, and no broader viewpoint on heterogeneity (modularity, coordination, dynamism) as described in this proposal has been published.

3.1.2 Modular Hardware and Energy Management for Heterogeneity

Going from a platform that can handle 1nW-10mW to one that can consume 1nW-500mW when on requires significant rethinking of concepts like core intermittent computing concepts like energy federation and management, task dispatching, and adaptation/approximation. A modular, general-purpose, energy-aware, and highly dynamic high-performance platform is needed to enable long-term, reliable deployments of batteryless devices. All intermittent computing research that builds real-world systems has used 16-bit MSP430s because of the on-board, directly addressable FRAM, enabling byte-level non-volatile storage and, therefore, faster, longer-lived checkpointing over FLASH. The Battery-free Game Boy (see Figure 5), built by the PI, is the first known to use ARM MCUs. This proposal envisions an ARM Cortex-M4 MCU that exposes its address/data bus, shared with diverse accelerator type components (FPGA, CNN), along with peripherals like sensors and radios. This bus is shared with high-speed non-volatile FRAM chip(s) for storing checkpoints and data across power failures. Energy harvesters and energy storage are reconfigurable at runtime, allowing for the platform to match peak power and energy storage to task demands and the level of energy available in the environment. Finally, multiple "signals" are embedded in the platform that informs adaptation and scaling. Figure 4, and Task 1 in Figure 1, shows the proposed modular platform architecture, where accelerator, harvester, and peripheral modules on a PCB can be "plugged/stacked" into the main board's shared bus.

Modularity and Heterogeneity. Embedded computing research platforms (and hobbyist like Arduino [3]) have a long history of modularity; including Epic Motes [22], and more recently Flicker [36]. Unlike previous approaches, the BFree platform must support a shared wide bus among multiple accelerators, sensors, peripherals, and memory elements. The microcontroller is the chief authority and is responsible for

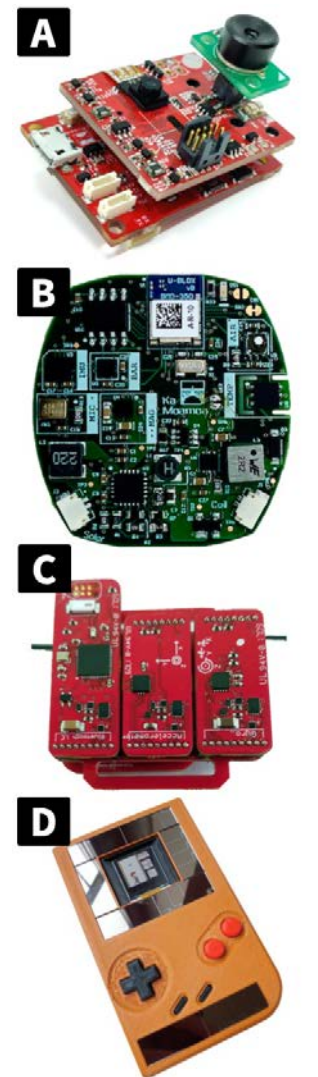


Figure 5: Platforms developed by the PI for battery-free computing: (A) FPGA vision platform, (B) smart face mask, (C) Flicker, (D) Battery-free Game Boy.

My CAREER Guided Tour

KA MOAMOA

Skipping ahead to Education and Outreach

Your proposal can die here!

This is an opportunity to do what you love!

Make it **personal**— you will love it and be **credible**

The proposed education plan outlines projects for K-12, PhD students, and the community. The keystone program of the plan will integrate battery-free and energy harvesting devices into a summer programming camp for K-8 Native Hawaiian students at Ke Kula Kaiapuni 'o Pū'ōhala School, a Hawaiian immersion bi-lingual public school. PI Hester is a Native Hawaiian, which along with other Indigenous people are grossly underrepresented in computing. PI Hester is the only Native Hawaiian Computer Engineering professor in the USA. It is the PIs goal to help prepare under-represented minority (URM) students, and especially Native Hawaiian/Indigenous students (who are often forgotten) as next-generation computing professionals through interrelated activities designed to develop critical computer science skills, and gain exposure to research.

camera when energy is abundant. Within these two modes, numerous other options exist, for example scaling the resolution or sample rate of the camera to reduce energy. When a program adapts, it's challenging to figure out the best thing to adapt, the impact on application quality, and what other alternatives or possibilities there might be. It's also hard to figure out how the energy environments and the richness thereof will affect the execution of different application paths or different adaptation levels.

We propose a tool for user-guided adaptation and application design exploration for heterogeneous intermittent computing systems. An interface presents an annotated task graph of the application. It provides estimates of application energy cost and execution statistics based on user-adjusted sliders, representing different program adaptation factors. These energy costs are partially gathered from static analysis of the code, with mappings to peripherals set up (or in the worst case a profiling conducted for discrete tasks). For each task, sliders map to knobs like sample rate, hidden layer depth, and allow the developer to immediately see the impact of changing mechanisms and degree of adaptation for the energy environments and hardware under test. A selection of energy harvesting environments and hardware configurations based on the BFree ecosystem will be available to select. We consider for the first time how FPGAs and CNN accelerators impact the performance and energy tradeoffs of intermittent computing in a design tool. With the tool, the designer can see the latency, energy, and memory costs for assigning a task to different computing entities. With the tool, the designer will map out fuzzy breakpoints for when computation must scale, either by going to a lower power computing element or reducing some "knob" like the sampling rate. This tool lets a developer map out a robust application that can handle multiple types of energy harvesting environments and situations. We will parameterize the BFree hardware platform and statically analyze code to build this simulation/emulation tool at compile time. While other approaches have investigated code profiling for speeding up runtime adaptation [16, 64], we leverage profiling and programmer specified inputs to understand the range of application quality possible in a tested environment.

3.4 Integration Task—Deployment in the Real World

The research proposal tasks, education and outreach activities are all integrated via real world deployment and testing. Demonstrating the generality of the proposed BFree framework is key to the evaluation, as environmental factors and real world issues can be road blocks to adoption.

We partner with health researchers, and community organizations to deploy prototype devices. We work with the SAGE project at Argonne National Lab to deploy a "green roof" stormwater management system with the Chicago Botanic Garden, enable wildlife surveillance on the coast and in urban prairies with The Nature Conservancy. We work with partners in Hawaii to deploy water monitoring sensors. We deploy mobile health devices like smart face masks, wrist worn activity trackers, and wearable cameras with researchers in the Feinberg School of Medicine at Northwestern. The work plan is shown in Figure 8.

| Tasks | 1 | 2 | 3 | 4 | 5 |
|-----------------------------------|---|---|---|---|---|
| (3.1) T1: Platform | | | | | |
| ↳ Hardware design | | | | | |
| ↳ Kernel development | | | | | |
| (3.2) T2: Language | | | | | |
| ↳ Sketchpoints | | | | | |
| ↳ Demonstrations | | | | | |
| (3.3) T3: Toolchain | | | | | |
| ↳ Adaptation Explorer | | | | | |
| ↳ Profiling/Modeling | | | | | |
| (3.4) T4: Integration | | | | | |
| ↳ major deployments with partners | | | | | |
| Distribution, Dissemination | | | | | |

Figure 8: Proposed work plan.

4 Education and Outreach Plan

The proposed education plan outlines projects for K-12, PhD students, and the community. The keystone program of the plan will integrate battery-free and energy harvesting devices into a summer programming camp for K-8 Native Hawaiian students at Ke Kula Kaiapuni 'o Pū'ōhala School, a Hawaiian immersion bi-lingual public school. PI Hester is a Native Hawaiian, which along with other Indigenous people are grossly underrepresented in computing. PI Hester is the only Native Hawaiian Computer Engineering professor in the USA. It is the PIs goal to help prepare under-represented minority (URM) students, and especially Native Hawaiian/Indigenous students (who are often forgotten) as next-generation computing professionals through interrelated activities designed to develop critical computer science skills, and gain exposure to research.

My CAREER Guided Tour

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K12 summer camps or engagement

Minority and historically underrepresented for bigger impact...

PhD student support, community STEM events, demo days, novel media...

Teaching a college class is not enough! You already do that for a living!

Context and Commitment. The PI is one of the founding members of the the Diversity Committee in the Computer Science Department at Northwestern, which has worked to establish summer programs for high school students starting in 2021, secured funding for 60 URM students to attend TAPIA Diversity Conference, and instituted a laptop loaner program for low income students. Finally, the PI is involved in multiple initiatives at the department, university, national, and global level to increase participation of Native Americans in STEM. Recently, the PI had a featured op-ed in Northwestern's alumni magazine titled "The World Needs Native Scientists Now," presented at a panel for the United Nations Department of Economic and Social Affairs on the intersection of Indigenous mindsets on sustainability and computing, and was awarded the Most Promising Engineer/Scientist by the American Indian Science and Engineering Society.

Sustainable Computing Summer Camp for Native Hawaiian Students. Unfortunately, most computing educational offerings are not relevant or engaging to Native Hawaiian students, as they do not map to the things that students care about. Computing is seen as esoteric and abstract. To address this gap, the PI will build and deploy culturally relevant physical computing curricula for Native Hawaiian students that are place-based, integrated with existing programs and partners in Kāne'ohe, Hawai'i, and reinforces learning Hawaiian culture and history alongside concepts of computer science. PI Hester works with a majority Native Hawaiian serving public school, that is taught in the Native Hawaiian language. PI Hester and collaborators at the school (Nelson, Sakai, and Plunkett) successfully piloted a summer camp in June of 2021 with 27 students who attended for two weeks (Figure 9). Students prototyped and programmed micro:bits using Microsoft Makecode, and learned about the ecology of the fishpond, conducting conservation activities and learning to code. The response from students was tremendous, with significant uptake of computer science concepts and positive feedback in surveys.



Figure 9: Native Hawaiian summer camp the PI piloted in June 2021 with Pū'ōhala School.

Future curriculum under the CAREER project will support students in understanding and exploring how they can use *energy harvesting* sensors (strongly related to the research), embedded systems, and wearables (via Makecode and micro:bits) to support natural resource preservation, health, art, and social skills in their community while respecting cultural norms related to sustainability. This effort will work to bridge the gap between sustainable computing efforts, novice-focused programming environments, and culturally appropriate technology integration within the environment. The CAREER will partially support some costs of the summer camp each year, including sensors and devices for programming. The summer program will also release asynchronous modules online, so that other students in the school can also participate, broadening the reach of the project. The Center for Native American and Indigenous Research Initiatives (CNAIR) at Northwestern (of which Hester is a member of the advisory board) has also agreed to participate. We hope to demonstrate the integration of Indigenous knowledge and computing, and build a pathway for recruiting native students into computing.

URM PhD Student Support and Video Interviews. The PI co-founded, advises and mentors URM PhD students in computing via a new group, Code' n' Color, which numbers 10-15 students and has been meeting weekly since April of 2020. The group meets weekly for coffee breaks and hosts URM PhD holders who are leaders in the computing industry and academia. The group is intended to provide a safe and supportive space for young scientists to interact with future faculty peers. Beyond the support group, he PI plans to design and host a website centered around the theme of the group, and to host / video record interviews with URM PhD holders to be published as "**Our Stories**" on the website. Leilani Battle from UMD, Valerie Taylor at Argonne, Chad Jenkins at Michigan, and Jelani Nelson at Berkeley, have already participated, and at least three other scientists have expressed interest. These will help raise the profile of minority PhD holders as well as give role models for URM computing students nationwide. The group also hosted a screening of "Coded Bias" documentary on facial recognition inaccuracies concerning black women,

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I did...

Sustainable Computing Summer Camp for Native Hawaiian Students.

URM PhD Student Support and Video Interviews.

Accessible Making with Go Baby Go!

and hosted the director for a campus-wide Q&A moderated by PI Hester.

Accessible Making with Go Baby Go! Since late 2018 the PI has been working with physical therapists and clinicians at Northwestern to augment toy ride on cars for children (ages 8 months to 4 years) with cerebral palsy and other mobility issues who either cannot afford a power wheelchair, or whose insurance has denied them. Mobility is key to general development both socially and physically, cars in GoBabyGo! support families and children using technology. In 2019 the PI helped build and deploy trackers for 12 cars and helped the team as technology consultant, with 12 families (Figure 10) in Chicago currently using the vehicles, in 2021 the PI helped deploy at least 20 cars. Going forward, the PI will integrate the GoBabyGo program into computer engineering curricula, allowing for the batteryless devices built in this proposal to be applied as interactive widgets for navigation, or as sensors to assist the parents and clinicians in understanding usage. The PI will provide a sign-up and recruitment process so students from classes at different levels (after undergoing training procedures on respectful engagement with families, children, and persons with a disability), can assist with the builds.



Figure 10: GoBabyGo!

Graduate and Undergraduate Classes. The PI teaches a seminar style Internet-of-Things course, and a wearables course. Components from the CAREER will be integrated into the course modules. It is envisioned that a module on energy harvesting and battery-free wearable devices will be developed for the Wearables course, and a dedicated module on heterogeneous intermittent computing for the seminar IoT class.

5 Broader Impacts

The proposed research will enable researchers, industry, and students to effectively use capable intermittently powered devices that harvest energy in real world applications. The results of this research will impact all fields where where long-term, low cost, massive scale sensing is essential including healthcare (wearable and body sensor networks), ecology, horticulture, agriculture, infrastructure and public utilities monitoring. Additionally, the work proposed here will enable a new class of heterogeneous intermittent computing devices, that promise as of yet unrealized new applications in the Internet-of-Things. If successful, this work will revolutionize how we build, test, and deploy these emerging systems. All hardware, software, and collected environmental profiles and energy traces will be made freely available to the research community in the appropriate venues, along with documentation and tutorials. Additionally, the platform, testbed, and tools will be made open and available to the community for evaluating new methodologies in energy harvesting devices, further aiding uptake and adoption by the community and enhancing research across the field. PI Hester's work has been well covered by the Wall Street Journal, BBC, CNET, The Verge, Seeker, Gizmodo, Engadget, Communications of the ACM, and many others, with over 20 million article impressions worldwide and 200,000 views on YouTube regarding PI Hester's research projects. This media attention helps to push broader audiences to focus on sustainability in computing.

6 Results From Prior NSF Support

CNS-1850496 CRII: CSR: Systems and Tooling Enabling Adaptive Intermittent Computing. (PI: Hester, 2/15/19 – 1/30/22; \$199,000) **Intellectual merit:** The project initiated exploration of energy-aware adaptation in intermittent computing on 16-bit microcontrollers. The goal was to enable efficient operation despite degraded performance. The CAREER proposal builds on these ideas and others, but reframes them in the context of heterogeneous computing. **Broader Impacts** The approaches will facilitate longer and reliable deployment of batteryless sensors. Impacts are a keynote lecture, ACM XRDS article, CACM article, and worldwide press on the battery-free Game Boy. *Publications:* [13, 18, 39, 49, 50, 81]. *Products:* Software and hardware artifacts for ASPLOS 2020 papers on timekeeping [19] and automatic checkpointing [51].

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Do what you're passionate about. Not a checkbox!

Best (?!) Practices (Or just ideas) – Community

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- **Mentoring**– senior mentors, and **peer** mentors. Need both! Different aims for each.
- Start a CAREER **writing group**– Zoom or local. Accountability is huge!
- Get **lunch, drinks, coffee**, with folks to talk about your ideas and get reactions. Dont throw any ideas away yet...



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Above all, you must find “Yes, and...” people

Best (?!) Practices (Or just ideas) – Ideation

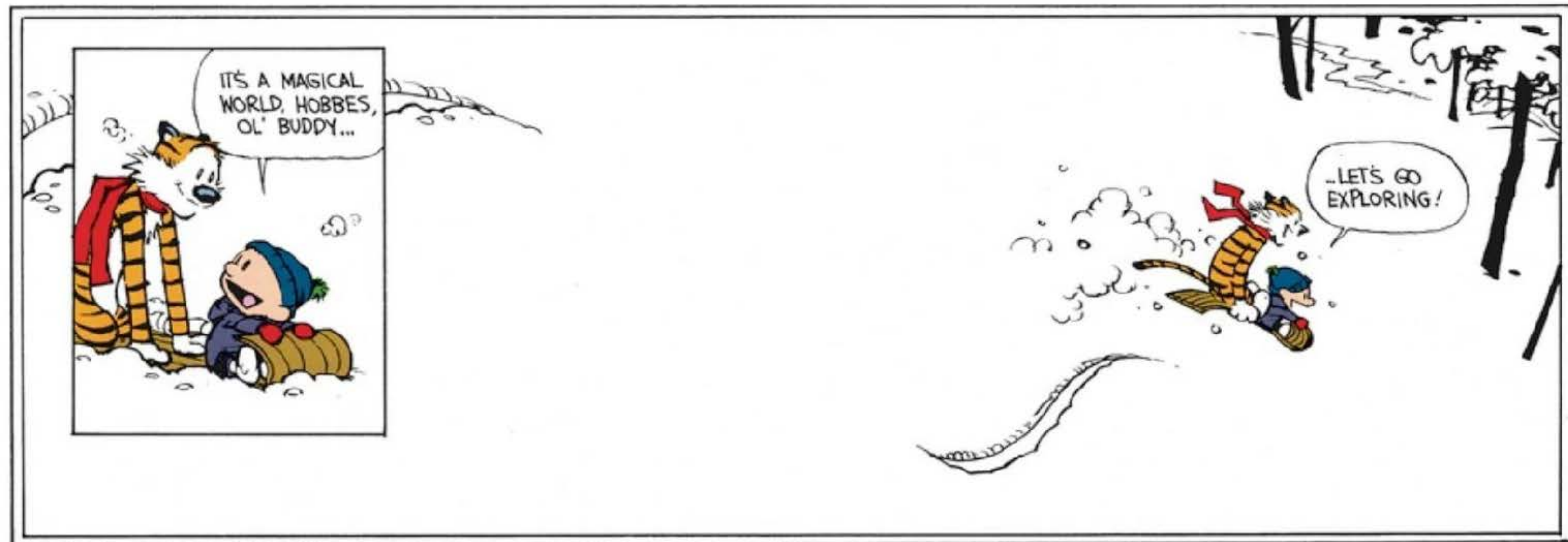
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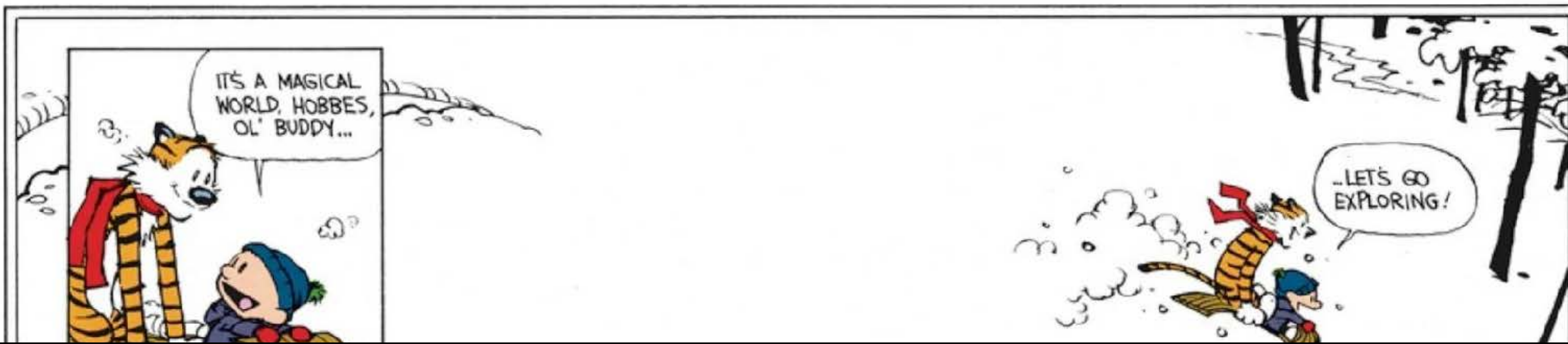
- Forced writing time. **Partition out the noise**—give yourself a dedicated slot.
- Unforced **creative** or mental health time!
(Walk in the woods, by the lake, hoop it up! Run!)
- Talk with your **students** and conduct deliberate, focused brainstorming.
- **START SUPER EARLY**





Give your ideas time to germinate and grow.





CAREER is an exploration– go enjoy it!

Good Luck! You can do it!

